

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0017] with the following amended paragraph:

[0017] **Figure 2** is a diagram of the internal components related to parallel processing of instructions in CPU 101 and the connection with system memory 105. CPU 101 includes a set of execution clusters 203A-203B, a fetch control unit 201, global reorder buffer (global ROB) 207 and a retirement unit 209. Fetch control unit 201 manages the retrieval of instructions to be executed by execution clusters 203A-203B from system memory 105. Fetch control unit 201 may also include an apportionment unit and cache. In one embodiment, fetch control unit 201 is a single device. In another embodiment, fetch control unit 201 is a set of devices such as a cache, memory access device and apportionment device. In a further embodiment, fetch control unit 201 manages the global order of fetches to memory 105. Fetch requests may be generated from fetch units in each execution cluster 203A-203B. A cache in fetch control unit 201 may be an instruction cache, trace cache or similar cache device. The cache in fetch control unit 201 stores instructions previously or recently retrieved from memory allowing fetch control unit 201 to retrieve instructions faster than if retrieved from memory 105. Multiple caches may also be used in fetch control unit 201 to optimize performance. In one embodiment, separate caches for instructions and segments (i.e., groupings of instructions including traces) may be used. ~~Caches for eaches caching~~ may be based on segments or traces that are built [by] based on repetition in the patterns of utilized instructions.

Please replace paragraph [0021] with the following amended paragraph:

[0021] In one embodiment, local reorder buffers 205A, 205B are each connected with a global reorder buffer 207. Global reorder buffer 207 tracks the relative order of instructions and segments in each local reorder buffer 205A, 205B. Output or ‘retirement’ device 209 uses the global reorder buffer to determine which execution cluster contains the next instruction or segment to be output to update the architecture of CPU 101 and computer system 100. In one embodiment, retirement unit 209 is a single device that retrieves data from execution clusters 203A, 203B and updates CPU 101 architecture and generates signals to computer system 100 components. In another embodiment, retirement unit 209 is a set of components that implement

the update of the architectural state. Global reorder buffer 207 also communicates with local reorder buffers 205A, 205B to update the local buffers when other execution clusters encounter mispredicted instructions. When a mispredicted instruction is encountered all instructions that were retrieved subsequent to the mispredicted instruction are erased or ‘flushed.’ A new set of instructions is then retrieved based on the actual resolution of the CTI that caused the misprediction. Global reorder buffer 207 works with local reorder buffers 205A and 205B to enforce a hierarchical distributed program reorder mechanism for CPU 101.

Please replace paragraph [0028] with the following amended paragraph:

[0028] In one embodiment, local reorder buffer B 205B notifies fetch control unit 201 of a mispredicted instruction via signal 307. The notification includes data identifying the instruction that had been mispredicted or the segment of the CTI that caused the misprediction. Fetch control unit 201 may utilize this data to fetch the correct instructions subsequent to the mispredicted CTI. In one embodiment, during the same time period that the misprediction of an instruction is detected in local reorders buffer B 205B retirement unit 209 retrieves the next segment of instructions to be implemented in CPU 101 architecture or to generate signals to computer system 100 components. In one embodiment, retirement unit 209 relies on data stored in the local reorder[s] buffers that tracks switch points in the assignment of segments to local reorder buffers. Retirement unit 209 uses this data to properly determine the order and location of instructions to be retired. In another embodiment, retirement unit 209 receives switch point data from the global reorder buffer 207. In the example, segment 1 is retired via signal 305. A retired local reorder buffer entry is then removed (i.e., deleted) from the local reorder buffer.

Please replace paragraph [0036] with the following amended paragraph:

[0036] **Figure 5** is a flowchart of a flush operation of global reorder buffer 207. In one embodiment, global reorder buffer 207 initiates a flush operation upon receipt of a misprediction notice from a local reorder buffer (block 501). Global reorder buffer 207 determines which switches stored in global reorder buffer 207 are subsequent to the segment that generated the misprediction (block 503). Global reorder buffer 207 sends a remote flush command to each local reorder buffer that has a segment entry that is indicated by a subsequent switch entry or a

segment entry that is subsequent to the segment indicated by the subsequent switch entry (block 505). Each switch entry that tracks a segment subsequent to the misprediction segment is marked to be flushed (block 507). A flush operation is then initiated to delete each entry marked for flushing from global reorder buffer 207 (block 509).